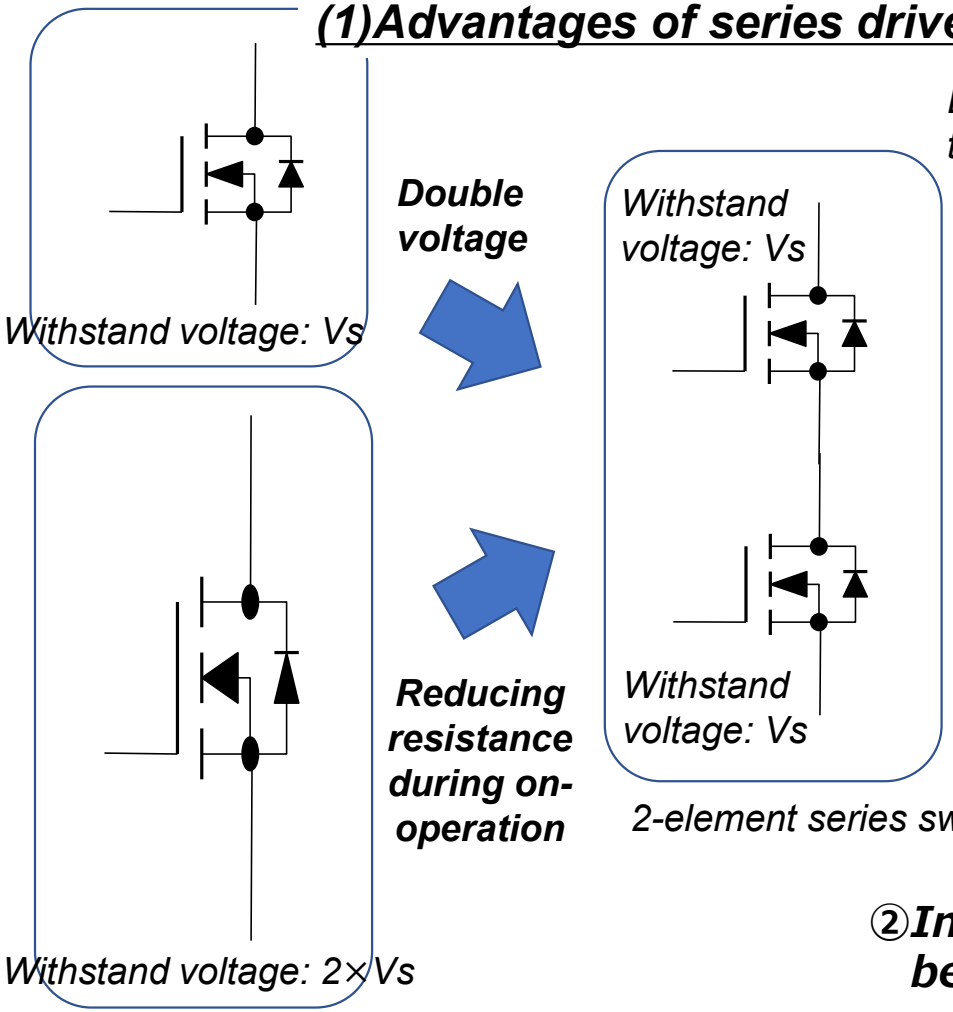
2. Research on drive technology for series-connected power semiconductor devices

①中西，浦壁，萩原，中嶋，檜垣，地道
「ゲート磁気結合方式を用いたSiC-MOSFET/SiC-SBDパワーモジュール直列駆動に関する研究」，電気学会半導体電力変換研究会，SPC-22-009/MD-22-009（2022）
②石井，浦壁，萩原，中嶋，檜垣，地道
「ゲート磁気結合トランスとコンデンサを併用したSiC-MOSFET/SiC-SBDスイッチング素子の直列駆動に関する研究」，2022年電気学会産業応用部門大会，1-40（2022）
③石井，神田，浦壁，萩原，糸川，檜垣，
「ゲート磁気結合トランスとコンデンサを併用したSiC-MOSFET/SiC-SBDスイッチング素子の直列駆動に関する研究」，電気学会半導体電力変換研究会，SPC-23-167（2023）
④神田，石井，浦壁，萩原，糸川，檜垣，
「ゲート磁気結合方式を用いた駆動回路におけるゲート電圧振動抑制方法」，電気学会 電子デバイス/半導体電力変換 合同研究会，EDD-23-029/SPC-23-212，2023
⑤神田，石井，浦壁，萩原，糸川，檜垣
「トランス並列ダンピング方式とコンデンサを併用した直列素子の電圧アンバランス抑制方法」，令和 6 年電気学会全国大会, 4-014（2024）

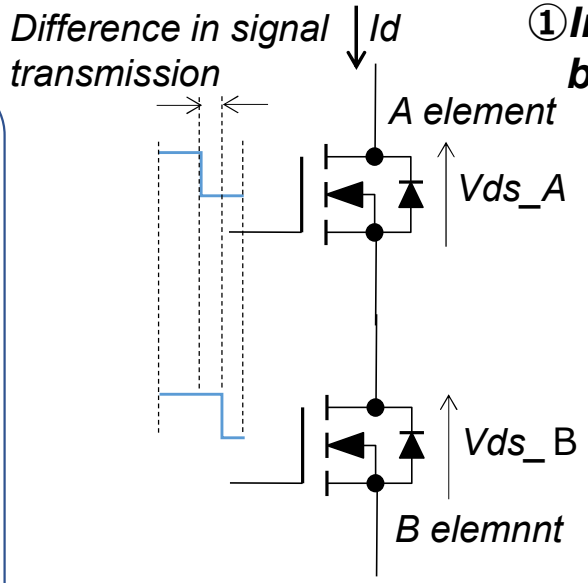
Purpose: Realizing of power semiconductor module series drive technology for low loss and low cost of power electronics equipment

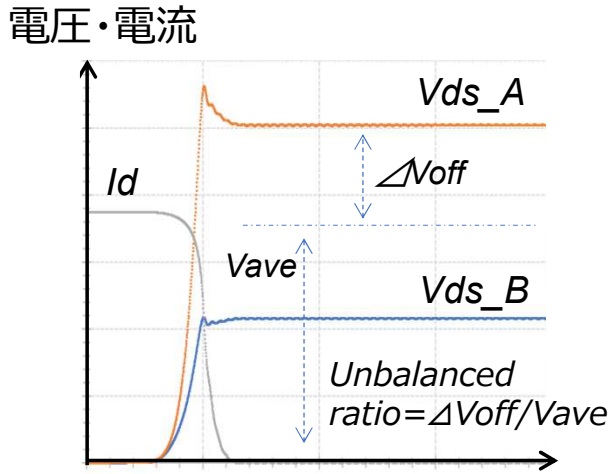
(1)Advantages of series drive



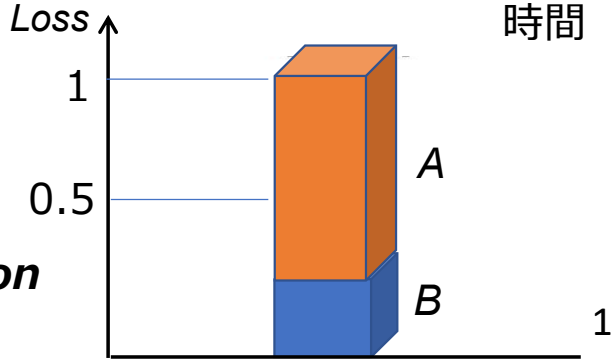
(2)Challenges of series drive

①Imbalance of applied voltage between elements



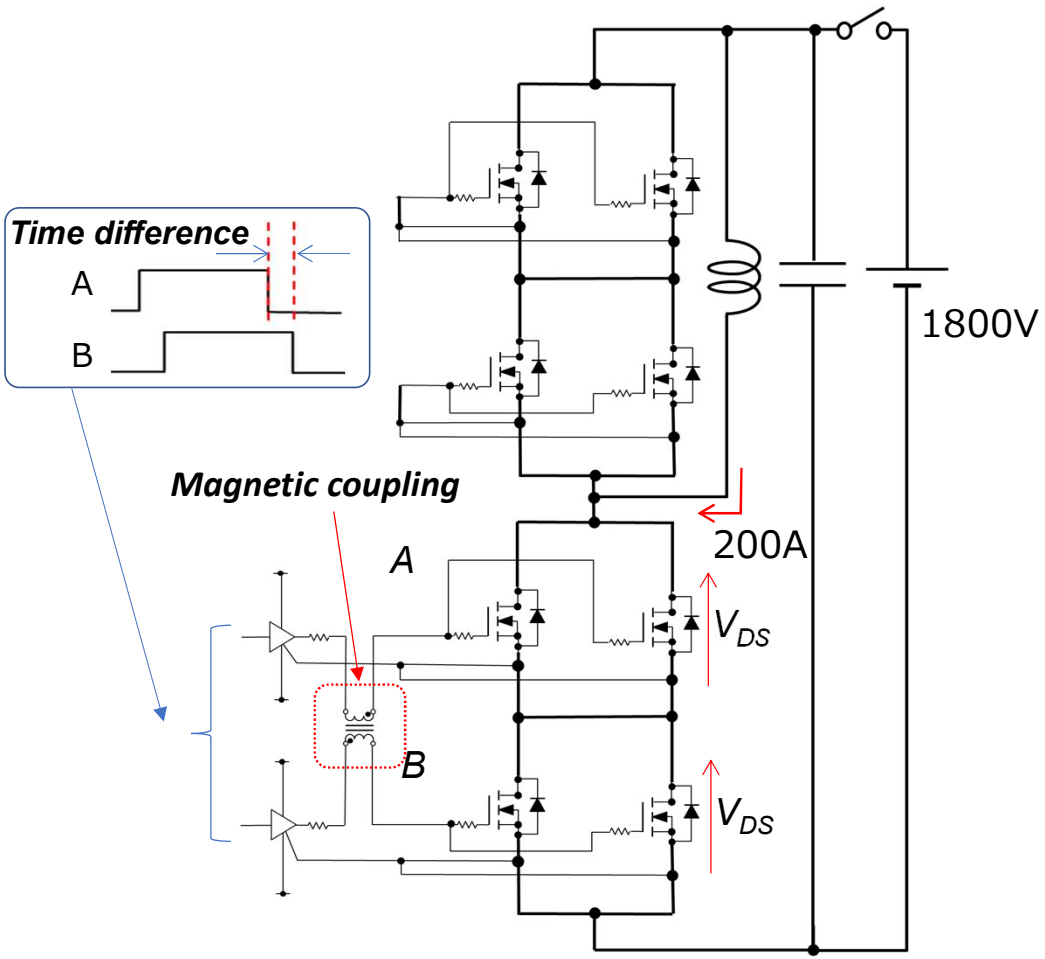


②Imbalance of heat generation between elements



- ✓ ***The gate magnetic coupling method (1) was selected to improve voltage imbalance during switching.***
- ✓ ***We proposed the following additions to the gate magnetic coupling method.***
  - ***①Damping gate drive method to suppress gate voltage oscillation without changing the switching speed.***
  - ***②Method of adding capacitor between DG terminals to improve VDS voltage imbalance.***
- ✓ ***The proposed method was validated in an experimental facility with 3.3 kV / 750 A SiC power modules in a 2-series, 2-parallel configuration.***

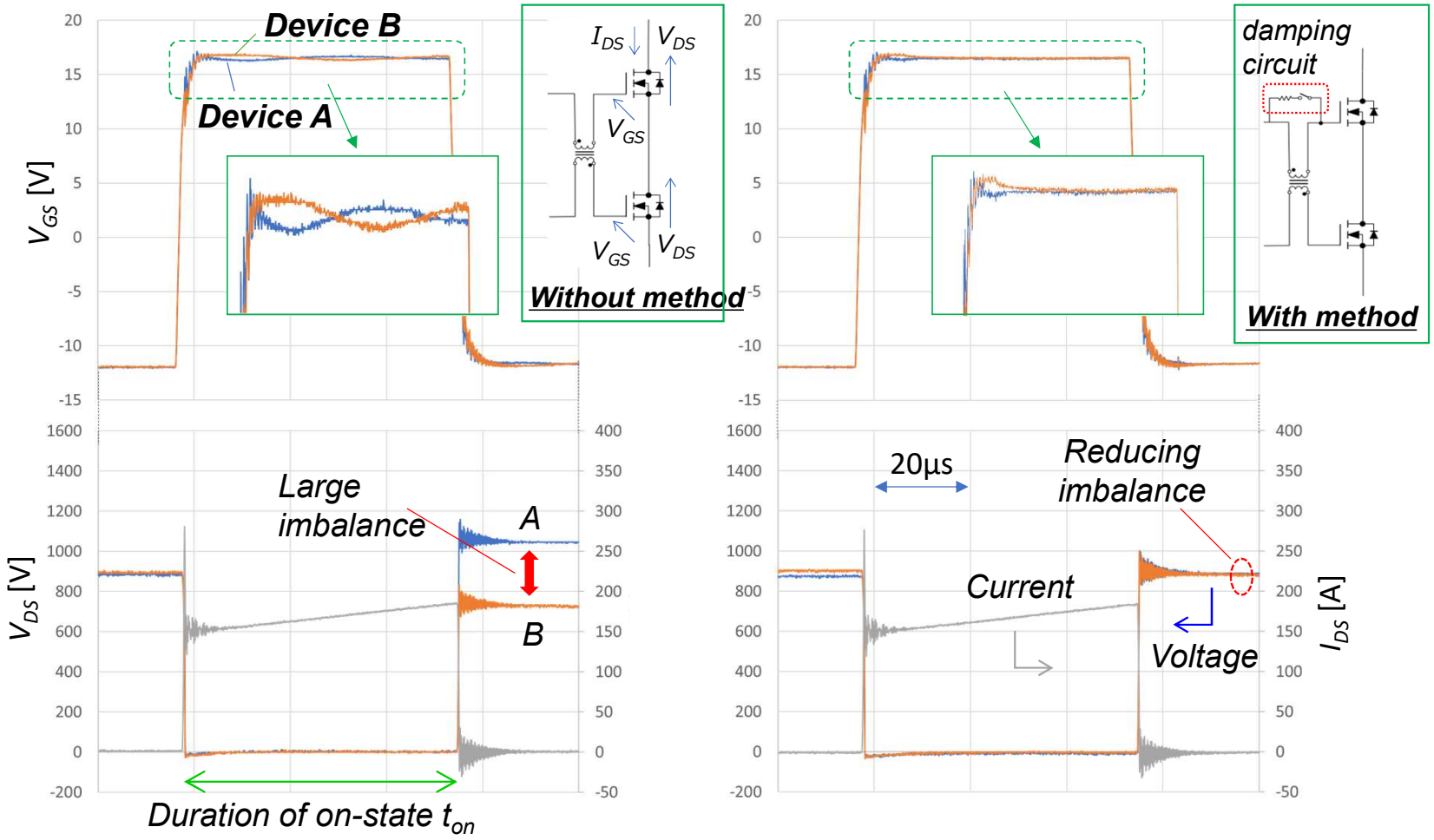
(1)Kiyoaki Sasagawa, Yasushi Abe, and Kouki Matsuse, "Voltage-Balancing Method for IGBTs Connected in Series", IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. 40, NO. 4, JULY/AUGUST 2004, 1025-1032 (2004)



3.3kV SiC power module 2-serial, 2-parallel configuration experimental facility

1. Proposal of Damping Gate Drive Method

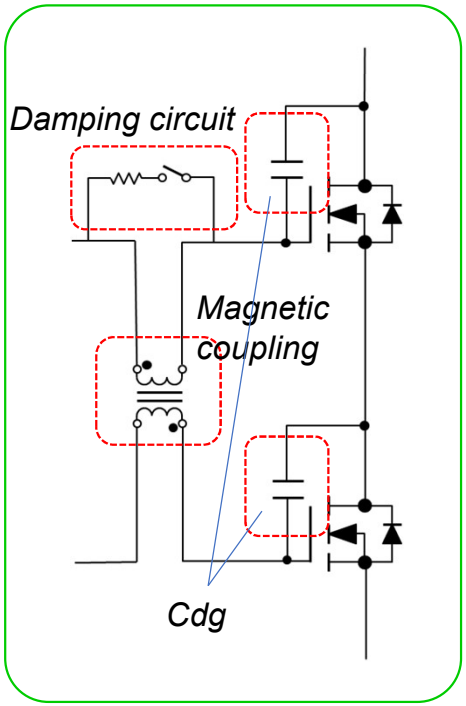
Damping gate drive method suppresses gate voltage oscillation and greatly reduces voltage imbalance.

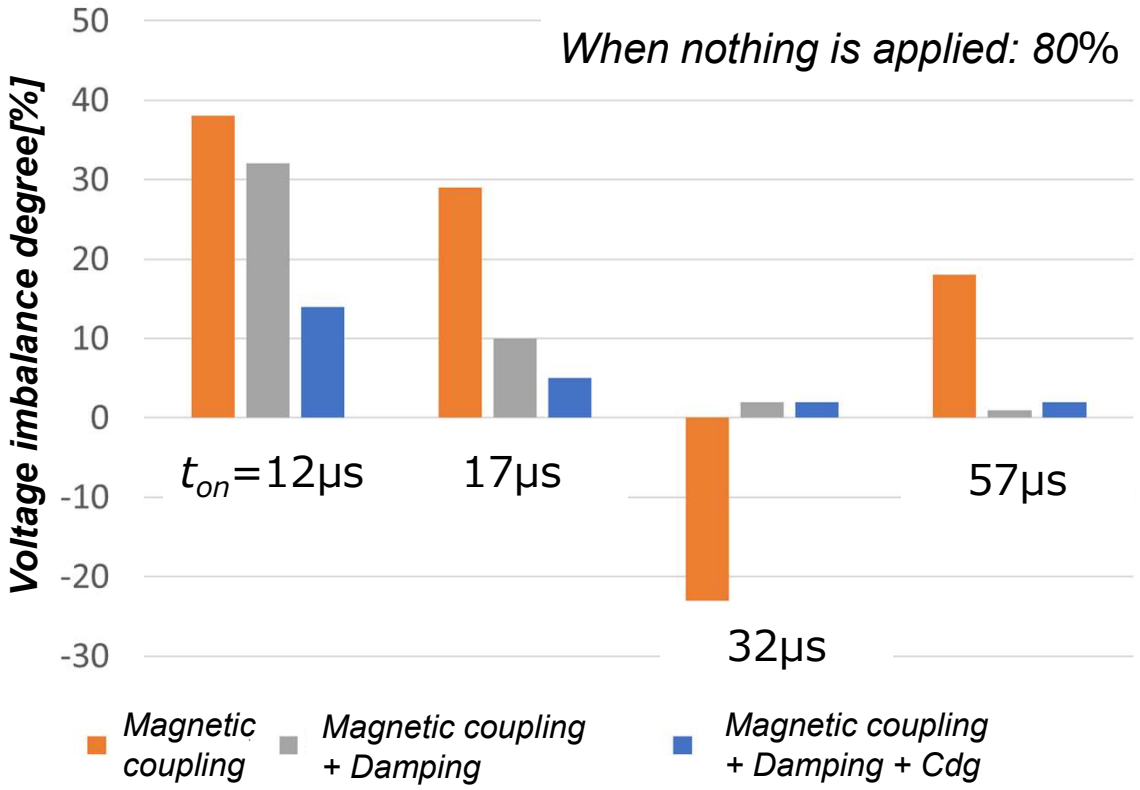


VGS, VDS, IDS waveforms without and with damping drive method (condition of gate signal time difference 150ns)

2. Propose of Magnetic coupling + damping gate drive + additional capacitor between DG terminals

Combination of damping gate drive method and adding a capacitor between DG terminals greatly improves voltage imbalance.





(Orange)
Due to gate voltage oscillation, magnetic coupling causes positive and negative voltage imbalance.
(Gray)
Damping method suppresses voltage imbalance.
(Blue)
Additional capacitors further improve voltage imbalance, especially in regions with short on-pulse widths.

Degree of voltage imbalance per on-pulse time t_{on} (condition of 150ns gate signal time difference)